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HIGH SPEED LOW VOLTAGE DIFFERENTIAL TO RAIL-TO-RAIL SINGLE ENDED CONVERTER

Field of the Invention

The present invention relates to converting a low voltage differential signal to a single ended signal, and, in particular, to a method and apparatus for converting a low voltage differential signal to a single ended signal using a trans-conductance amplifier that is arranged in cooperation with a trans-impedance stage.

Background of the Invention

Low Voltage Differential Signaling (hereinafter referred to as LVDS) is a technology used in data transmission systems. In LVDS, data is transmitted over two wires as a low voltage differential signal, with half of the differential signal on each wire. A low voltage differential signal typically has peak-to-peak amplitudes in the range from 250mV to 450mV. Since LVDS is a differential signaling method, the LVDS signal does not have an absolute reference level. The low voltage swing minimizes power dissipation, while maintaining high transmission speeds. Typical transmission speeds are over 100 Mbps (Mega-bits per second).

Brief Description of the Drawings

Non-limiting and non-exhaustive embodiments of the present invention are described with reference to the following drawings.

FIG. 1 is an illustration of an example embodiment of a circuit for converting a differential low-voltage signal into a single-ended signal;

FIG. 2 is an illustration of another example embodiment of a circuit for converting a differential low-voltage signal into a single-ended signal;

FIG. 3 illustrates yet another example embodiment of a circuit for converting a differential low-voltage signal into a single-ended signal, using a rail-to-rail implementation; and

FIG. 4 is an illustration of still another example embodiment of a circuit for converting a differential low-voltage signal into a single-ended signal, arranged in accordance with aspects of the present invention.

Detailed Description of the Preferred Embodiment

Various embodiments of the present invention will be described in detail with reference to the drawings, where like reference numerals represent like parts and assemblies throughout the several views. Reference to various embodiments does not limit the scope of the invention, which is limited only by the scope of the claims attached hereto. Additionally, any examples set forth in this specification are not intended to be limiting and merely set forth some of the many possible embodiments for the claimed invention.

Throughout the specification and claims, the following terms take at least the meanings explicitly associated herein, unless the context clearly dictates otherwise. The meanings identified below are not intended to limit the terms, but merely provide illustrative examples for the terms. The meaning of "a," "an," and "the" includes plural reference, the meaning of "in" includes "in" and "on." The term "connected" means a direct electrical connection between the items connected, without any intermediate devices. The term "coupled" means either a direct electrical connection between the items connected or an indirect connection through one or more passive or active intermediary devices. The term "circuit" means either a single component or a multiplicity of components, either active and/or passive, that are coupled together to provide a desired function. The term "signal" means at least one current, voltage, charge, temperature, data, or other signal.

Briefly stated, the invention is related to a method and system that converts a differential low-voltage input signal (e.g. LVDS or RSDS) into a single-ended output signal. An operational trans-conductance amplifier (OTA) is configured to convert the input signal into a current. A trans-impedance stage is configured to convert the current into the single-ended output signal. The voltage associated with the output of the OTA corresponds to approximately VDD/2. The trans-impedance stage comprises an inverter circuit, a p-type transistor, and an n-type transistor. The

transistors are arranged in a negative feedback configuration with the inverter. The single-ended output signal has a voltage swing that approximately corresponds to the sum of the V_{GS} of the n-type transistor and the V_{GS} of the p-type transistor. The output signal may be buffered by additional circuits such as an inverter, a Schmitt trigger, as well as others.

FIG. 1 is an illustration of an example embodiment of a circuit (100) for converting a differential low-voltage signal into a single-ended signal that is arranged in accordance with aspects of the present invention. Circuit 100 comprises an OTA (110) and a trans-impedance stage (120). An example OTA 110 comprises a current source (130) and transistors (M1-M4). Trans-impedance stage 120 comprises an inverter circuit (Inv1) and transistors (M5-M6).

Transistor M1 has a gate that is coupled to node N152, a drain that is coupled to node N160, and a source that is coupled to node N164. Transistor M2 has a gate that is coupled to node N150, a drain that is coupled to node N162, and a source that is coupled to node N164. Transistor M3 has a gate that is coupled to node N162, a drain that is coupled to node N160, and a source that is coupled to node N158. Transistor M4 has a gate that is coupled to node N162, a drain that is coupled to node N162, and a source that is coupled to node N158. Transistor M5 has a gate that is coupled to node N154, a drain that is coupled to node N158, and a source that is coupled to node N160. Transistor M6 has a gate that is coupled to node N154, a drain that is coupled to node N156, and a source that is coupled to node N160. Current source 130 is coupled between nodes N156 and N164. Inverter circuit Inv1 has a first input that is coupled to node N160 and an output that is coupled to node N154.

Circuit 100 is arranged to operate as follows below. A first supply signal (VSS) is applied at node N158, and a second supply signal (VDD) is applied at node N156. An input signal (Vdiff) is applied across nodes N150 and N152. Signal Vdiff corresponds to a differential signal (e.g. LVDS or RSDS). Signal Vdiff comprises a first half (Vinp) and a second half (Vinn) such that Vinp-Vinn=Vdiff, where Vinp is applied at node N150 and Vinp is applied at node N152.

Transistors M1 and M2 are arranged to operate as a differential pair. Transistors M3 and M4 are arranged in a current mirror configuration. The trans-impedance circuit is configured to maintain node N160 at approximately VDD/2 (halfway between the power supply rails). Current source 130 is configured to provide a tail current (Itail) for the differential pair at node N164. OTA 110 is arranged to provide an intermediate current (I_O) from node N160 to trans-impedance stage 120 in response to the differential signal (Vdiff). Current I_O is approximately given by I_O = Vdiff * $gm_{1,2}$.

Trans-impedance stage 120 is configured to provide an output signal (OUT) at node N154 in response to current I_O. Trans-impedance stage 120 is further configured to servo the voltage associated with node N160 (VOUTB) to approximately VDD/2 such that inverter circuit Inv1 is biased at a mid-supply level. Accordingly, inverter circuit Inv1 is configured to operate as a trans-impedance amplifier. Trans-impedance stage 120 is arranged such that transistor M5 is active when current I_O is positive, and transistor M6 is active when current I_O is negative. Transistors M5 and M6 are arranged to operate as source followers when active. The voltage associated with signal OUT (VOUT) is approximately given by: VOUT = VDD/2 + VGS_5 when I_O is positive, and VOUT = VDD/2 + VSG_6 when I_O is negative. Accordingly, the voltage swing associated with signal OUT corresponds to VGS_5 + VSG_6. In one example, (VGS_5 + VSG_6) corresponds to approximately 1.8 V, and the voltage range associated with the power supplies is up to 2.5 V, and the circuit can directly drive a normal inverter. For power supplies greater than 3.0 V the circuit may be followed by an inverter with hysteresis.

The speed associated with operation of circuit 100 is adversely impacted by a parasitic capacitance (Cpar1) that is present at node N160. Changes in the voltage associated with node N160 is given by: $\Delta V = I_O * \Delta t$ / Cpar1. Accordingly, the time (Δt) required to discharge node N160 is given by Δt = Cpar1*$\Delta V/I_O$. VOUTB is maintained at an approximately constant level such that ΔV is small. Accordingly, circuit 100 is configured to perform conversion of the logic levels from differential to single-ended at high speeds.

Inverter circuit Inv1 is biased approximately in the middle of the power supply rails (VDD, VSS). The sizes of the transistors in inverter circuit Inv1 are selected such that the quiescent current in Inv1 is within a tolerable limit, and is capable of driving the gate capacitance associated with transistors M5 and M6, as well as any subsequent circuits.

FIG. 2 is an illustration of another example embodiment of a circuit (200) for converting a differential low-voltage signal into a single-ended signal that is arranged in accordance with aspects of the present invention. Circuit 200 comprises an OTA (210), a trans-impedance stage (120), and a buffer circuit (230). An example buffer circuit 230 comprises an inverter circuit (Inv2). An example OTA 210 comprises current sources (130, 220, and 222) and transistors (M1-M4). Trans-impedance stage 120 comprises an inverter circuit (Inv1) and transistors (M5-M6).

Transistor M1 has a gate that is coupled to node N152, a drain that is coupled to node N160, and a source that is coupled to node N164. Transistor M2 has a gate that is coupled to node N150, a drain that is coupled to node N162, and a source that is coupled to node N164. Transistor M3 has a gate that is coupled to node N162, a drain that is coupled to node N160, and a source that is coupled to node N156. Transistor M4 has a gate that is coupled to node N162, a drain that is coupled to node N162, and a source that is coupled to node N156. Transistor M5 has a gate that is coupled to node N154, a drain that is coupled to node N158, and a source that is coupled to node N160. Transistor M6 has a gate that is coupled to node N154, a drain that is coupled to node N156, and a source that is coupled to node N160. Current source 130 is coupled between nodes N158 and N164. Current source 220 is coupled between nodes N158 and N162. Current source 222 is coupled between nodes N158 and N160. Inverter circuit Inv1 has an input that is coupled to node N160 and an output that is coupled to node N154. Inverter circuit Inv2 has an input that is coupled to node N154 and an output that is coupled to node N250.

Circuit 200 is configured to operate in a substantially similar manner as circuit 100. OTA 210 includes an n-type differential pair instead of a p-type differential

pair. Also, circuit 200 includes an optional buffer circuit (230) and two additional current sources (220, 222) that are not shown in FIG. 1.

Current source 220 is configured to provide current at node N162. When the polarity of the differential input signal (Vinp, Vinn) changes, transistor M2 becomes inactive and the voltage at node N162 is pulled to VDD by M4 and parasitic leakage. When the differential input signals (Vinp, Vinn) change polarity again, transistor M4 will not operate properly until a parasitic capacitance (Cpar2) associated with node N162 is charged. Current source 210 is configured to provide current at node N162 to maintain a charge on the parasitic capacitance (Cpar2). By maintaining a charge on the parasitic capacitance (Cpar2), operation of circuit 200 is enhanced and prevented from slowing down. Current source 222 is configured to provide a current at node N160 that matches the current provided by current source 220 at node N158, such that offset in the OTA is minimized.

The buffer circuit (e.g., Inv2) is configured to provide a buffered output signal (OUT2B) in response to the output signal (OUT). As discussed previously with respect to FIG. 1, the output signal (OUT) has a voltage swing that corresponds to VGS_5+VSG_6. Buffer circuit 230 is arranged to improve the rail-to-rail performance of the buffered output signal (OUT2B). Buffer circuit 230 also provides additional gain to the output. One example buffer circuit (230) comprises an inverter. Another example comprises an even number of inverters couple together in series such that the output is non-inverting with respect to node N154. Yet another example comprises an odd number of inverters couple together in series such that the output is inverting with respect to node N154. Still another example buffer circuit (230) comprises a Schmitt trigger, as illustrated in FIG. 2. The quiescent current that is associated with the buffer circuit (230) may be reduced when the Schmitt trigger is used.

FIG. 3 illustrates yet another example embodiment of a circuit (300) for converting a differential low-voltage signal into a single-ended signal, using a rail-to-rail implementation, which is arranged in accordance with aspects of the present invention. Circuit 300 comprises a first OTA (110), a second OTA (210), and a trans-impedance stage (120). Circuit 300 operates in a substantially similar manner as circuit

100 and circuit 200. OTA 110 is configured to operate with a common mode voltage that is in the range from VSS to (VDD - VDS_7 - VSG_1). OTA 210 is configured to operate with a common mode voltage that is in the range from VDD to (VSS + VDS_7' + VGS_1'). By including OTA 110 and OTA 210, rail-to-rail performance of circuit 300 is enhanced.

Circuit 300 illustrates an example embodiment where circuit Inv1 comprises a NAND gate (N1). The first input of NAND gate N1 is coupled to node N160, while the second input is coupled to an ENABLE signal. NAND gate N1 is configured such that power is conserved when signal ENABLE is deactivated.

FIG. 4 is an illustration of still another example embodiment of a circuit (400) for converting a differential low-voltage signal into a single-ended signal that is arranged in accordance with aspects of the present invention. Circuit 100 comprises an OTA (110), trans-impedance stage (120), an inverter circuit (Inv2), current source (220 and 222), and a bias circuit (410). An example bias circuit (410) includes transistors (Mb1-Mb3). An example OTA 110 comprises a current source (130) and transistors (M1-M4). Trans-impedance stage 120 comprises an inverter circuit (Inv1) and transistors (M5-M6). An example of inverter circuit Inv1 includes transistors (M8-M9). An example of inverter circuit Inv2 comprises transistors (M10-M11). An example of current source 130 comprises a transistor (M7). An example of current source 220 comprises a transistor (Mb4). An example of current source 222 comprises a transistor (Mb5).

Transistor M1 has a gate that is coupled to node N152, a drain that is coupled to node N160, and a source that is coupled to node N164. Transistor M2 has a gate that is coupled to node N150, a drain that is coupled to node N162, and a source that is coupled to node N164. Transistor M3 has a gate that is coupled to node N162, a drain that is coupled to node N160, and a source that is coupled to node N158. Transistor M4 has a gate that is coupled to node N162, a drain that is coupled to node N162, and a source that is coupled to node N158. Transistor M5 has a gate that is coupled to node N154, a drain that is coupled to node N158, and a source that is coupled to node N160.

Transistor M6 has a gate that is coupled to node N154, a drain that is coupled to node N156, and a source that is coupled to node N160. Transistor M7 has a gate that is coupled to node N440, a drain that is coupled to node N164, and a source that is coupled to node N156. Transistor M8 has a gate that is coupled to node N160, a drain that is coupled to node N154, and a source that is coupled to node N156. Transistor M9 has a gate that is coupled to node N160, a drain that is coupled to node N154, and a source that is coupled to node N158. Transistor M10 has a gate that is coupled to node N154, a drain that is coupled to node N250, and a source that is coupled to node N156. Transistor M11 has a gate that is coupled to node N154, a drain that is coupled to node N250, and a source that is coupled to node N158.

Transistor Mb1 has a gate that is coupled to node N440, a drain that is coupled to node N442, and a source that is coupled to node N156. Transistor Mb2 has a gate that is coupled to node N150, a drain that is coupled to node N440, and a source that is coupled to node N442. Transistor Mb3 has a gate that is coupled to node N152, a drain that is coupled to node N440, and a source that is coupled to node N442. Transistor Mb4 has a gate that is coupled to node N440, a drain that is coupled to node N162, and a source that is coupled to node N156. Transistor Mb5 has a gate that is coupled to node N440, a drain that is coupled to node N160, and a source that is coupled to node N156.

Circuit 400 is configured to operate in a substantially similar manner as circuit 100. Bias circuit 410 is configured to enhance the common mode voltage (VCM) range of circuit 400. As the common mode voltage changes, the VDS of M7 changes. To accurately mirror the current from Mb1 to M7 their VDS's must match. Mb2 and Mb1 maintain the VDS of Mb1 equal to M7. This maintains the current through M7 at the proper value even if M7 goes out of saturation at high common mode voltages

The above specification, examples and data provide a complete description of the manufacture and use of the composition of the invention. Since many embodiments of the invention can be made without departing from the spirit and scope of the invention, the invention resides in the claims hereinafter appended.